

200Gb/s QSFP56 DR4 Transceiver

QSFP56-200G-DR4

Features

- Hot-pluggable QSFP56 form factor
- Built-in 200G PAM4 DSP
- Supports 212.5Gb/s aggregate bit rates
- Low power dissipation < 5.5W
- Commercial case temperature range of 0°C to 70°C
- Single 3.3V power supply
- Maximum link length of 500m over SMF
- Uncooled 4 channels 1310nm EML
- 4 channels PIN photo detector array
- 200GAUI-4 electrical interface
- Single MPO12 receptacle
- CMIS V4.0 compliant
- Built-in digital diagnostic functionality

Applications

- IEEE 802.3bs 200GBASE-DR4 Ethernet (PAM4)
- Data center

Description

Optone's QSFP56-200G-FR4 200GE QSFP56 Optical Transceiver modules are designed for using in 200 Gigabit Ethernet links over single-mode fiber. They are compliant with the QSFP MSA and with IEEE 802.3bs 200GBASE-DR4 specification. Digital diagnostics functions are available via the I2C interface as specified by CMIS V4.0.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V_{cc}	-0.3	3.6	V
Input Voltage	V_{in}	-0.3	$V_{cc}+0.3$	V
Storage Temperature	T_s	-20	85	°C
Case Operating Temperature	T_c	0	70	°C
Humidity (non-condensing)	Rh	5	95	%

Recommended Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit
Supply Voltage	V_{cc}	3.13	3.3	3.47	V
Operating Case Temperature	T_c	0		70	°C
Baud Rate per Lane (PAM4)	fd		26.5625		GBaud/s
Power Dissipation	P_m			5.5	W
Fiber Bend Radius	R_b	3			cm

Electrical Specifications

Parameter	Symbol	Min	Typical	Max	Unit
Differential Input Impedance	Z_{in}	90	100	110	ohm
Differential Output Impedance	Z_{out}	90	100	110	ohm
Differential Input Voltage Amplitude	ΔV_{in}	300		900	mVpp
Differential Output Voltage Amplitude	ΔV_{out}	300		900	mVpp
Bit Error Rate ^{Note}	BER			2.4E-4	
Input Logic Level High	V_{IH}	2.0		V_{cc}	V
Input Logic Level Low	V_{IL}	0		0.8	V
Output Logic Level High	V_{OH}	$V_{cc}-0.5$		V_{cc}	V
Output Logic Level Low	V_{OL}	0		0.4	V

Note

1.Compliant with 200GBASE-DR4 electrical specification in IEEE802.3bs standard.

Optical Characteristics

Parameter	Symbol	Min	Typical	Max	Unit
Transmitter					
Center Wavelength	λ_c	1304.5		1317.5	nm
Side-mode suppression ratio	SMSR	30			nm
Average Launch Power (each lane)	P_{out}	-5.1		4	dBm
Launch power in OMA_{outer} minus TDECQ	P_{tdecq}	-4.4			dBm
Transmitter and dispersion eye closure (each lane)	TDECQ			3.4	dB
Average launch power of off transmitter(each lane)	P_{off}			-30	dBm
Outer Extinction Ratio	ER	3.5			dB
Optical Return Loss Tolerance	ORLT			21.4	dB
Receiver					
Center Wavelength	λ_c	1304.5		1317.5	nm
Damage threshold	R_{dam}	4			dBm
Average Receive Power (each lane) Input (each lane)	P_{in}	-8.1		3	dBm
Receiver Power (OMA_{outer}) (each lane) ^{Note}	OMA_{out}			2.8	dBm
Stressed Receiver Sensitivity (OMA_{outer}) (each lane)	Sens			-4.1	dBm
Receiver Sensitivity (OMA_{outer}) (each lane) ^{Note}	Sen			-6.6	dB

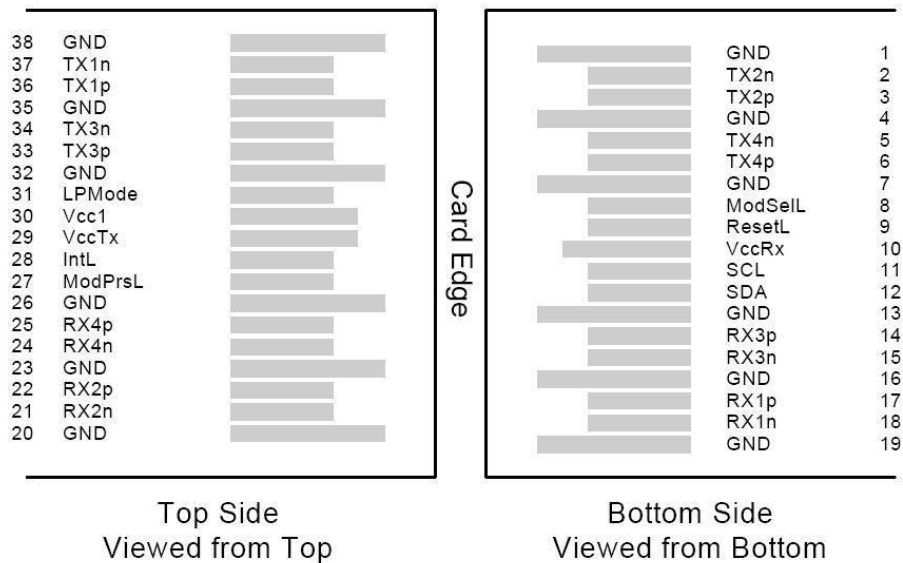
Note:

1. Measured with conformance test signal at TP3 for the BER specified in section 138.1.1 of IEEE 802.3cd.

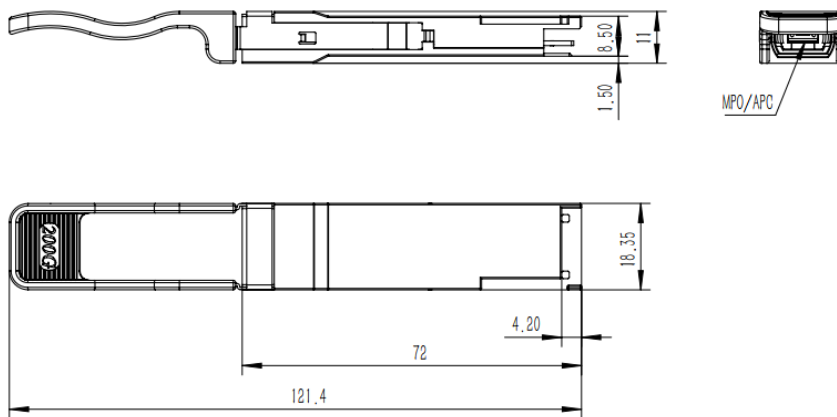
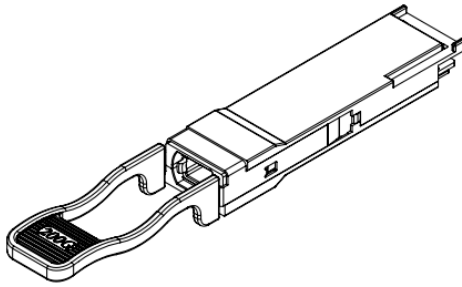
Pin Description

Pin	Logic	Symbol	Name/Description
1		GND	Module Ground
2	CML-I	Tx2-	Transmitter inverted data input
3	CML-I	Tx2+	Transmitter non-inverted data input
4		GND	Module Ground
5	CML-I	Tx4-	Transmitter inverted data input
6	CML-I	Tx4+	Transmitter non-inverted data input
7		GND	Module Ground
8	LVTTTL-I	MODSEIL	Module Select
9	LVTTTL-I	ResetL	Module Reset
10		VCCR _x	+3.3V Receiver Power Supply
11	LVC MOS-I	SCL	2-wire Serial interface clock
12	LVC MOS-I/O	SDA	2-wire Serial interface data
13		GND	Module Ground
14	CML-O	RX3+	Receiver non-inverted data output
15	CML-O	RX3-	Receiver inverted data output
16		GND	Module Ground
17	CML-O	RX1+	Receiver non-inverted data output

18	CML-O	RX1-	Receiver inverted data output
19		GND	Module Ground
20		GND	Module Ground
21	CML-O	RX2-	Receiver inverted data output
22	CML-O	RX2+	Receiver non-inverted data output
23		GND	Module Ground
24	CML-O	RX4-	Receiver inverted data output
25	CML-O	RX4+	Receiver non-inverted data output
26		GND	Module Ground
27	LVTTTL-O	ModPrsL	Module Present, internal pulled down to GND
28	LVTTTL-O	IntL	Interrupt output, should be pulled up on host board ²
29		VCCTx	+3.3V Transmitter Power Supply
30		VCC1	+3.3V Power Supply
31	LVTTTL-I	LPMODE	Low Power Mode
32		GND	Module Ground
33	CML-I	Tx3+	Transmitter non-inverted data input
34	CML-I	Tx3-	Transmitter inverted data input
35		GND	Module Ground
36	CML-I	Tx1+	Transmitter non-inverted data input
37	CML-I	Tx1-	Transmitter inverted data input
38		GND	Module Ground



Mechanical Specifications



Ordering Information

Part Number	Product Description
QSFP56-200G-DR4	QSFP56, 200GBASE-DR4 Transceiver, 500m over SMF, MPO

Important Notice

Performance figures, data and any illustrative material provided in this data sheet are typical and must be specifically confirmed in writing by OPTONE before they become applicable to any particular order or contract. In accordance with the OPTONE policy of continuous improvement specifications may change without notice.

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Edition OCT 16, 2023
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